Project profile

Cluster for Application and Technology Research in Europe on NanoElectronics

CA501 | Communication-centric heterogeneous multi-core architectures (COMCAS)

PROJECT CONTRIBUTES TO

Communication	✔
Automotive and transport	
Health and aging society	
Safety and security	
Energy efficiency	✔
Digital lifestyle	
Design technology	✔
Sensors and actuators	
Process development	
Manufacturing science	✔
More than Moore	
More Moore	✔
Technology node	

TECHNOLOGY PLATFORM FOR PROCESS OPTIONS

Partners:

ATRENTA
AXIOM-IC
CEA-LETI
CEA-LIST
MARVELL
NXP Semiconductors
Recore Systems
ST Ericsson
STMicroelectronics
SYNOPSYS
Thales
TIMA
TUD
UCLM
Uni Nice-Sophia Antipolis
UPV

Project leader:

Armand Castillejo
ST Ericsson

Key project dates:

Start: March 2009
End: March 2010

Countries involved:

France
The Netherlands
Spain

A strong consortium of European semiconductor industries, academics and small and medium-sized enterprises has combined skills in the CATRENE COMCAS project to address the challenge of finding a breakthrough in ultra-low-power design for data-communication-centred, heterogeneous, multicore architectures, targeting 45 nm and 32 nm CMOS technologies. These architectures will be exploited in a number of future applications and particularly in the next generation of mobile phones and mobile multimedia entertainment devices. This CATRENE project is looking at all aspects of minimal power design, blending semi- and full-custom circuit designs at transistor level in technologies of 45 nm and beyond.

In the coming years, mobile electronic equipment will require more cores with an estimated increase of 1.4 times a year, working at higher frequencies – increasing at 1.05 times a year – and with a resultant increase in power consumption. However, the growth of battery capacity at only 5% a year will not be sufficient to guarantee the autonomy of embedded systems.

There is a marked trend towards heterogeneous platforms which include sophisticated on-chip communications infrastructures for higher efficiency and performance. Moreover, heterogeneous cores provide a solid balance between performance and power consumption. The CATRENE CA501 COMCAS project will generate a breakthrough in ultra-low-power design solutions for new heterogeneous platforms – crucial in view of the growing complexity of mobile communications and multimedia equipment.

The only way to maintain European leadership in this vast and demanding worldwide market is to invest in architectures that enable new features and that have distinguishing characteristics such as low-power consumption.

Time for change

From the system architecture and integration perspective, the challenge is in determining the types of architecture that are needed to satisfy the application and market requirements. Most major personal computer manufacturers are now using embedded devices and are shifting to multiple cores on a single chip to improve processor performance.

Increasing the processor clock rate has been the popular technique for increasing processing speed for over 30 years. However, that approach is now running out of steam, due to excessive power consumption, heat dissipation – needing a fan which adds cost and generates noise – and electromigration-related reliability issues.

Furthermore, using aggressive voltage-scaling techniques to reduce power consumption, combined with multiple clock domains, increases the susceptibility of the system to various noise sources. In addition, variability of technical parameters, voltages and temperature as well as manufacturing defects will affect the reliability and performance of devices implemented in 45 nm and 32 nm CMOS technology. Reliability is also affected by accelerated ageing of circuits with soft errors induced by alpha particles and neutrons and atmospheric interference.

Consequently, the implementation of fault tolerance in advanced integrated circuits becomes necessary and will be mandatory to keep yield at an acceptable value. However, fault tolerance has major disadvantages, such as a significant increase in power dissipation. On the other hand,

low consumption is a major requirement in portable multimedia devices and digital entertainment systems.

Using new architecture

Currently, there are only a few players who can manage the entire system design effort alone. These facts guide the players to find appropriate partnerships to solve the existing design or productivity bottlenecks. The goal of COMCAS is to reduce power consumption by a factor of five while at least maintaining the performance of today's systems. The main innovation is to change the traditional performance-oriented design approach to an integral power-performance approach for a configurable communication-centred heterogeneous multicore architecture.

Key elements of this integral approach are:

- Communication centred, run-time configurable, heterogeneous multicore hardware/software;
- Advanced power management at platform level;
- High-level power estimator tools with an accuracy to within 20% of the real energy costs; and
- Innovative electronic design automation flow and tools.

Thanks to hardware/software configurability, such a versatile architecture is able to target several product derivatives based on the same silicon – such as different standards in different market regions – or can guarantee the reuse of the same architectural platform and intellectual properties across different product generations. Moreover hardware/software configurability will simplify the way to power down dynamically all components that are not necessary at a given time for a specific application scenario – for example by an advanced power-management strategy.

Tackling leakage current

Previously, dynamic power was the dominant source for power consumption. However, with future deep sub-micron technologies, the leakage current – or static power – can no longer be neglected. In newer technologies, static power will become dominant over dynamic power so the possibility of reusing area-by-time multiplexing the same silicon for different driver software package (DSP) kernels becomes more and more important.

This cannot be achieved with an application-specific integrated circuit. COMCAS will therefore use other programmable architectures – such as coarse-grained reconfigurable hardware, field-programmable gate arrays and DSPs – to achieve area reuse. The target is that area reuse will lead to an overall 40% reduction in system power.

A communication-centred architecture will improve overall communications efficiency among heterogeneous cores and facilitate better productivity for derivative designs, because of the interoperability capabilities of integrating IP or processor cores using different protocols.

The importance of dynamic voltage and frequency scaling is well known. However, individual clocking of components often leads to practical difficulties in communications between components. In this project, issues of synchronisation, as well as crossing clock domains, are investigated to solve these inter-component communications problems which result from clock scaling. The target is a 30% overall power reduction of the system resulting from new communications concepts.

Setting Europe apart

To ensure a leading position in this huge mass market, new ultra low-power architectures for multi-standard multi-media devices are an absolutely essential requirement. There is no doubt that consumers will continue buying portable electronic devices. However, Europe has to distinguish itself from Asian vendors in terms of features and low-power advantages in order to maintain a leading position.

Europe has long been a pioneer in mobile devices. However, competition is heavy and comes mainly from Asian manufacturers. They rapidly encroach on the market whenever innovation ceases because of their lower production costs. That is why it is of prime importance for Europe to maintain a high level of innovation in the area through co-operative R&D.

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CATRENE (Σ! 4140), the EUREKA **C**luster for **A**pplication and **T**echnology **R**esearch in **E**urope on **N**ano**E**lectronics, will bring about technological leadership for a competitive European information and communications technology industry.

CATRENE focuses on delivering nano-/microelectronic solutions that respond to the needs of society at large, improving the economic prosperity of Europe and reinforcing the ability of its industry to be at the forefront of the global competition.